Meeting 7: 2/3/2015: Register Allocation

Announcements
HW3 due 2/14
- two weeks!

HW2 Comments

- Understanding and debugging PLY+++++++++
- Getting started on own
- Submitted test cases that go against spec+ -- let us know
- LALR(1)
- Multiline statements
- Reserved words
- Shift/reduce conflicts+
- Regex+
- Hard to build incrementally
- Thinking of edge cases++

Time Spent

- 3.8 hours mean, 6 hours median,
- How hard 3.0 mean, 4 median (out 6)

Questions

HW3 - Register Allocation

Current compilers - all vars on the stack

but slow!

Register - 1 cycle, cache in tens
Memory - hundred thousands
the most important compiler optimization

x86: 8 registers

- spilling

9 variables live at the same time

x = \ldots

\underbrace{x} \quad \text{live}

x = \ldots

or live at a location if it is read at a later location with no intervening assignments
HW3

Flatten AST ➔ Instrucr selection ➔ x86 IR

x86 IR ➔ Register Allocation ➔ x86 IR w/ registers

\[
\begin{align*}
  x &\rightarrow \%eax \\
  y &\rightarrow \%ebx \\
  z &\rightarrow \%eax
\end{align*}
\]

not live at the same time or hold same value

Live-ness Analysis ➔ Build interference graph ➔ Graph coloring

interfere

edges: vars that interfere — have overlapping live ranges

color this graph